PATENT
DOCKET NO.: 2207/9865
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	Manoj Khare et al.
SERIAL NO.	:	09/749,660
FILED	:	December 28, 2000
FOR	:	METHOD AND APPARATUS FOR REDUCING MEMORY LATENCY IN A CACHE COHERENT MULTI-NODE ARCHITECTURE
GROUP ART UNIT	:	2186
EXAMINER	:	Tuan V. Thai
ASSIGNEE	:	INTEL CORPORATION

HON. COMMISSIONER
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PRELIMINARY AMENDMENT

S I R:

Please enter the following amendment prior to examination of the present application